

A Method for Making Nanoscale Wires and Gaps for Switches and Transistors**ABSTRACT**

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A method for forming first and second linear structures of a first composition that meet at right angles, there being a gap at the point at which the structures meet. The linear structures are constructed on an etchable crystalline layer having the first composition. First and second self-aligned nanowires of a second composition are grown on this layer and used as masks for etching the layer. The self-aligned nanowires are constructed from a material that has an asymmetric lattice mismatch with respect to the crystalline layer. The gap is sufficiently small to allow one of the structures to act as the gate of a transistor and the other to form the source and drain of the transistor. The gap can be filled with electrically switchable materials thereby converting the transistor to a memory cell.

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